# Improved RF Modeling Techniques for Enhanced AlGaN/GaN HFETs

S. Nuttinck, E. Gebara, J. Laskar, J. Shealy, and M. Harris

***Abstract*—Modeling procedures of an AlGaN/GaN HFET that incorporate the effects of both a GaN cap layer and an AlN subbuffer layer are presented. A single off-state measurement method to extract all eight parasitic elements of an enhanced HFET has been successfully applied. In addition, procedures to model the nonlinear drain-to-source current characteristics featuring a kink are described.**

***Index Terms*—AlGaN/GaN HFETs, nonlinear modeling, small-signal modeling.**

## I. Introduction

AlGaN/GaN HFETs offer important advantages for high-power microwave applications such as phased array antennas and base stations [1], [2]. Different GaN-based device structures are being considered and researched to improve the transistors reliability and performance. This paper focuses on devices in which a GaN cap layer, and an AlN subbuffer layer have been added to the HFET layer structure with the objective to improve the gate-drain breakdown voltage [3], and the GaN buffer layer quality [4]–[7], respectively. In the studied HFET, the modifications result in a steady kink in the current characteristics. The AlN subbuffer layer is sometimes attributed to be at the origin of this feature [8]. Since an accurate model is essential to fully benefit from the device's high performance in circuit design, parameters extraction and modeling procedures that integrate the effects of the cap-layer and of the subbuffer layer must be implemented. When modeling a device high-frequency and nonlinear characteristics, a precise extraction of its parasitic elements is critical since it influences the determination of the intrinsic elements values. The conventional Cold-FET method [9], [10] used for on-wafer parasitic elements de-embedding requires forward and reverse bias small-signal measurements, as well as a relation for unequivocal determination of the resistive elements. Because of the GaN cap layer, forward biasing the studied AlGaN/GaN HFET's results in a high gate-to-source polarization leading to more delicate extraction procedure. We propose in this paper to extract all eight parasitic elements from a single off-state ($V_{GS} < V_{TH}$, $V_{DS} = 0$ V) measurement. This technique simplifies the modeling procedures and does not require forward biasing. Very good agreement between the measured and the simulated small-signal parameters have been obtained using this modeling method without a final tuning routine. Also, procedures to model the nonlinear current characteristics (kink) are presented.

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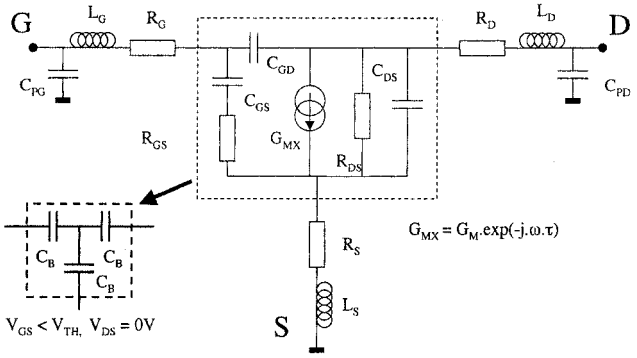


Fig. 1. HFET equivalent circuit model.

In Section II the improved method for parasitic elements extraction is successfully applied in the small-signal modeling of an enhanced AlGaN/GaN HFET, and, Section III presents the innovative technique to model the device nonlinear current characteristics featuring a kink.

## II. Enhanced Device Structure

The studied transistors are 12-finger devices with a total gate width of 1.5 mm and a gate length of 0.3 $\mu$m, resulting in a cutoff frequency above 40 Ghz. A 50 Å thick GaN cap layer is grown on top of the AlGaN barrier to decrease the gate leakage and improve the breakdown characteristics [3]. Also a 200 nm thick AlN subbuffer layer is grown between the SiC substrate and the GaN buffer to reduce the stress due to lattice mismatch and improve the GaN crystal quality. This results in better device performance and reliability [5]. Power densities in the X-band above 10 W/mm have been reported using similar structures [11].

## III. Improved RF Modeling Method

A standard Hybrid-Pi topology (Fig. 1) is used to simulate the small-signal characteristics of an AlGaN/GaN HFET (gate width = 1.5 mm) from 1 GHz to 12 GHz. The elements outside the dotted box represent the extrinsic part of the device. They result from the metal traces and the probing pads.

The method to extract all eight parasitic elements combines the reversed Cold-FET procedure [10], and an LDMOS modeling technique [10]. The "active" part of a pinched-off FET at $V_{DS} = 0$ V is a depleted region that can be modeled by a

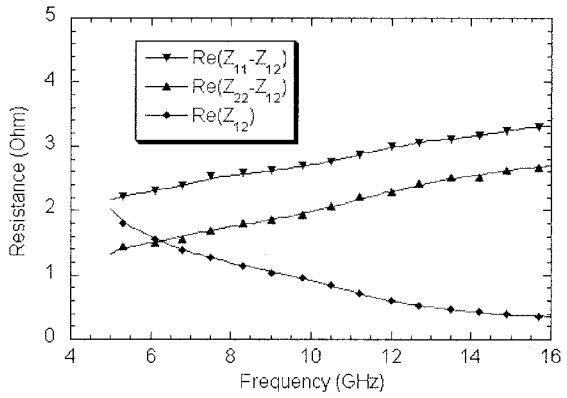


Fig. 2. Extraction procedure for the determination of the resistive parasitic elements values.

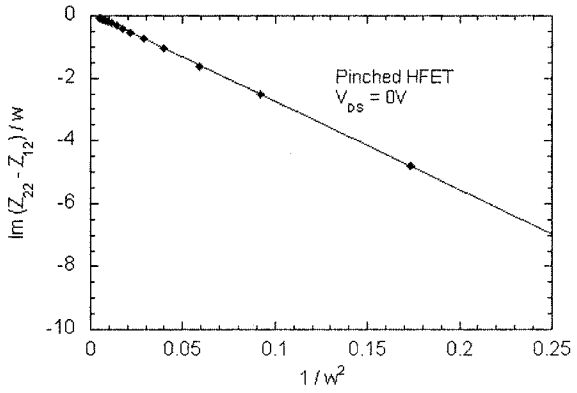


Fig. 3. Extraction procedure for the determination of the inductive parasitic elements values.

symmetric capacitive network (Fig. 1) [11], [12]. This results in simple expressions for the imaginary part of the device's $Y$-parameters that are used to extract the pad capacitances ($C_{PG}$ and $C_{PD}$) [10]. These parasitic capacitances are de-embedded from the measured $Y$-parameters, which are converted to $Z$-parameters. These $Z$-parameters contain the contribution of the parasitic inductive ($L_S$, $L_G$, $L_D$) and resistive ($R_S$, $R_G$, $R_D$) elements, as well as the contribution of the depletion region. They can be expressed through [12]

$$\begin{aligned} Z_{11} - Z_{12} &= R_G + j.\omega.L_G - \frac{j}{\omega.C_B} \\ Z_{22} - Z_{12} &= R_D + j.\omega.L_D - \frac{j}{\omega.C_B} \\ Z_{12} &= R_S + j.\omega.L_S - \frac{j}{\omega.C_B} \end{aligned} \quad (1)$$

where the capacitor $C_B$ describes the total depletion capacitance under the gate. The real part of these quantities is used to determine the parasitic resistances ($R_S$, $R_G$, $R_D$) (Fig. 2), and the imaginary part is used for parasitic inductive elements ($L_S$, $L_G$, $L_D$) extraction (Fig. 3). In Fig. 2, the measured characteristics to determine the values of the access resistances exhibit a constant drift with frequency of $\pm 0.1\ \Omega$/GHz. The resistances values are extracted in the middle of the frequency range.

All 8 parasitic elements being determined, the intrinsic elements can be calculated at any bias points from the intrinsic

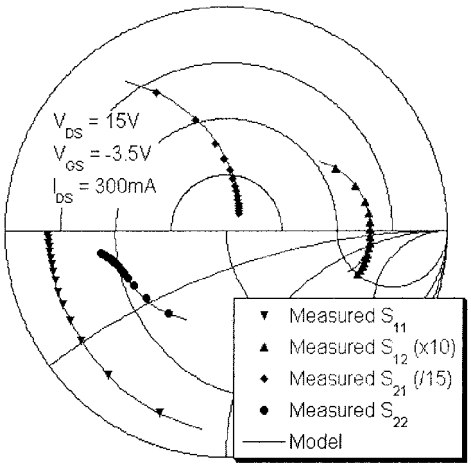


Fig. 4. Comparison between modeled and simulated results from 1 to 12 GHz.

$Y$-parameters [10], [13]. For the studied device, the extracted parasitic elements are 51 fF, 36 fF, 2.7 Ω, 2 Ω, 0.9 Ω, 65 pH, 71 pH, and 0.2 pH, for $C_{PD}$, $C_{PG}$, $R_G$, $R_D$, $R_S$, $L_G$, $L_D$, and $L_S$, respectively. The coherency of the method is confirmed by the good agreement between the measured and simulated $S$-parameters (Fig. 4).

## IV. Nonlinear Current Modeling

In applications where $f_T$ is well above the frequency of operation, the device current-voltage characteristics dominate its nonlinear behavior [14], making the modeling of the channel current critical for accurate simulation. Nonlinear drain-to-source current ($I_{DS}$) are commonly modeled by [15]

$$I_{DS} = \left( \sum_{k=1}^{3} g_k \cdot (V_{GS} - V_{TH})^k \right) \cdot \tanh(\alpha \cdot V_{DS}) \quad (2)$$

where the polynomial terms contain information about pinch-off and $I_{DS}$ saturation. For $V_{GS}$ corresponding to an open channel away from saturation, only the first order term is considered. In this case the device $I_{DS}(V_{DS})$ characteristics featuring a kink (Fig. 6) can be modeled by considering a bias-dependent threshold voltage ($V_{TH}$)

$$I_{DS} = g_0 \cdot (V_{GS} - V_{TH}(V_{DS}, V_{GS})) \cdot \tanh\left( \frac{V_{DS}}{\delta(V_{GS})} \right) \quad (3)$$

where $g_0$ is a parameter with the units of conductance, and $\delta(V_{GS})$ is a linear relation that defines the knee of the current characteristics. The case $V_{TH}(V_{DS}, V_{GS}) = V_{TH}^0 = const$ corresponds to kink-free current characteristics. By fitting to (3) the part of the current characteristics where $V_{TH}$ is constant (part of the $I_{DS}(V_{DS})$ curves on the left side of the kink) it is possible to extract parameters $g_0$, $\delta(V_{GS})$, and $V_{TH}^0$. Then, subtracting these modeled kink-free characteristics to the measured kinked current characteristics, modeled with (3), leads to the expression of $V_{TH}(V_{DS}, V_{GS})$

$$V_{TH}(V_{DS}, V_{GS}) = V_{TH}^0 - \frac{\Delta I_{DS}}{g_0 \cdot \tanh\left( \frac{V_{DS}}{\delta(V_{GS})} \right)} \quad (4)$$

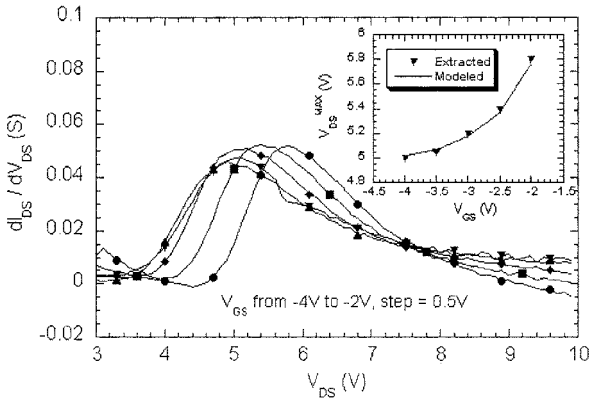


Fig. 5. $dI_{DS}/dV_{DS}$ at various $V_{GS}$ for $V_{DS}^{\mathrm{MAX}}$ determination, and extracted and modeled $V_{DS}^{\mathrm{MAX}}$ parameter.

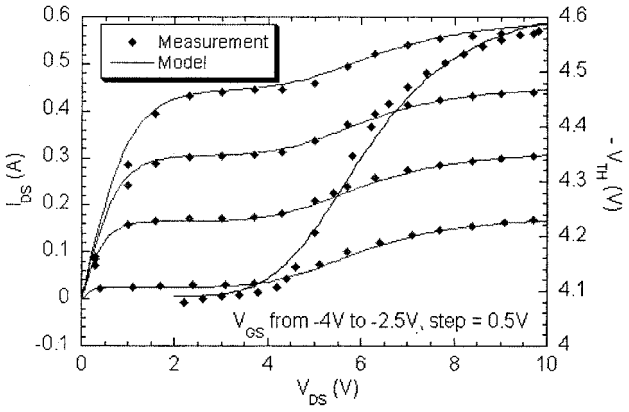


Fig. 6. Measured and modeled drain-to-source current characteristics.

where $\Delta I_{DS}$ is the difference between the measured current characteristics (with kink) and the modeled current curves (without kink). Bias-dependent $V_{TH}$ has an asymmetrical step shape (Fig. 6), and can be modeled by

$$V_{TH}\left(V_{DS}, V_{GS}\right) = V_{TH}^{0} + \frac{\Delta V_{TH}}{1+\exp\left(-\frac{V_{DS}-V_{kink}(V_{GS})}{\rho(V_{DS})}\right)} \tag{5}$$

where $\Delta V_{TH}$ expresses the maximum variation of $V_{TH}$, $V_{kink}$ determines the position of the step relatively to the drain bias, and $\rho(V_{DS})$ controls how asymmetric the step is. The variation of $V_{kink}(V_{GS})$ is similar to the variation of the drain voltage $V_{DS}^{\max}(V_{GS})$ that maximizes $(dI_{DS}/dV_{DS})$. In Fig. 5 we observe that the kink starts at higher values of $V_{DS}$ when increasing the gate bias. Finally, $V_{kink}$ is modeled with

$$V_{kink}(V_{GS}) = \alpha + V_{DS}^{\max}(V_{GS}) = \alpha + A + B\cdot\exp\left(\frac{V_{GS}-C}{D}\right). \tag{6}$$

Best fits were obtained for $\alpha = 1$V, $A = 4.95$ V, $B = 0.8$ V, $C = -2$ V, $D = 0.8$ V. $\rho(V_{DS})$ is modeled using a linear relation. An optimization routine gives $\Delta V_{TH} = -0.55$ V, and $\rho(V_{DS}) = 0.24 + 0.14 * V_{DS}$.

Fig. 6 shows extracted and modeled data for the threshold voltage. Finally the model of the threshold voltage is used to calculate the drain current using (3). The simulated current characteristics agree well with the measured data over the bias range where self-heating is not dominant (Fig. 6).

The fitting equations used in the model not only accurately predict the drain-to-source current characteristics, but enable derivation with respect to $V_{GS}$ and $V_{DS}$, that is crucial for prediction of the fundamental frequency, of the harmonics generation, and of the power added efficiency, under large signal operation.

## V. Conclusion

A single off-state measurement method that does not require any current flowing between the gate and the source has been successfully applied to accurately extract all the parasitic elements in equivalent circuit RF modeling of an enhanced AlGaN/GaN HFET. In addition, procedures to model the nonlinear drain-to-source current characteristics featuring a kink are described.

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